

# **Obey The LAW**

## **Put Your Enterprise on Intel Architecture**

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**Patrick P. Gelsinger**

Vice President / Chief Technology Officer  
Intel Corporation

Federal Office Systems Expo  
Washington D.C.  
March 19, 2002



***..doubling the  
transistor density  
every 18-24 months..***

**MOORE'S LAW**

# The Last 30 Years

## Exponential Compute Performance

Performance



**1 MPH**



**10 MPH**

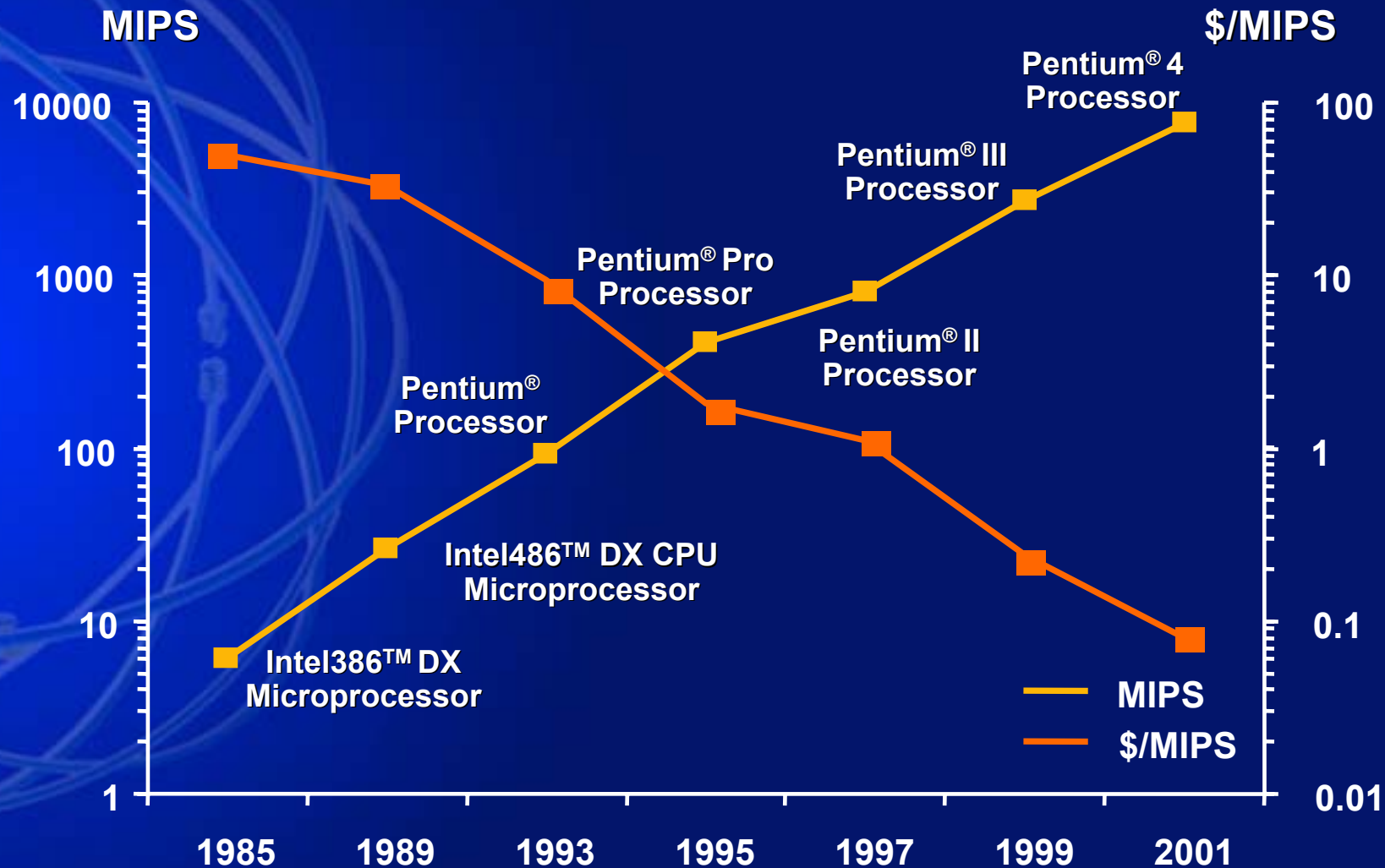


**1000 MPH**

1970 1980 1990 2000 2010 2020

# Intel Architecture

## Obeying the LAW



# The Result

**1000x** *the performance of a*  
**\$1M** *mainframe in a*  
**\$1K** *desktop in*  
**30** *years ...*



The background is a blue-tinted collage of various Intel-related images and text. It includes a large circular graphic in the center, a desktop monitor, a laptop, a calculator, and several Intel processor boxes. Text elements like 'IA-32', 'INTEL ITANIUM PROCESSOR FAMILY', 'INTEL INSIDE', 'INTEL PERSONAL INTERNET CONNECTED ARCHITECTURE', and 'INTEL EXCHANGE ARCHITECTURE' are scattered throughout. The main text is centered over the circular graphic.

***Foundational  
building blocks  
and solutions for  
the entire industry***

# Intel® Pentium® 4 Processor Family



- Designed for compute intensive applications, e.g.
  - Multimedia
  - Communications & cryptography
- Designed for MHz headroom – **10+ GHz !**

**Industry-leading IA-32 Price/Performance**

# Performance Clients for Today's Enterprise Clients



**Enabling New Applications In The Enterprise**

**Demo**

[www.intel.com/labs](http://www.intel.com/labs)

**Intel Labs**



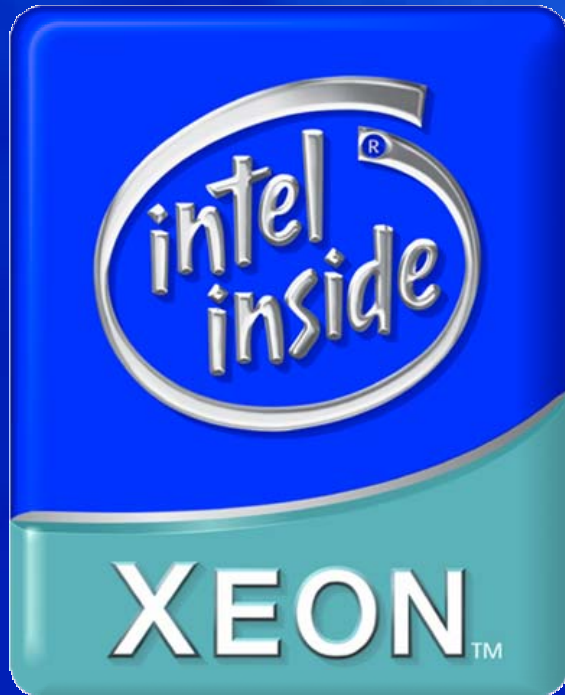
# Intel® Pentium® 4 Processor-M Family



- Designed for optimal
  - Performance
  - Battery life
  - Wireless connectivity
  - Form factors

**Addressing Mobility Needs For Business**

# Intel® Xeon™ Processor Family



- Designed to meet high-performance computing needs
- Industry-leading price/performance
- Deployed in mission critical platforms

**Continuing Innovation on the IA-32 Family**

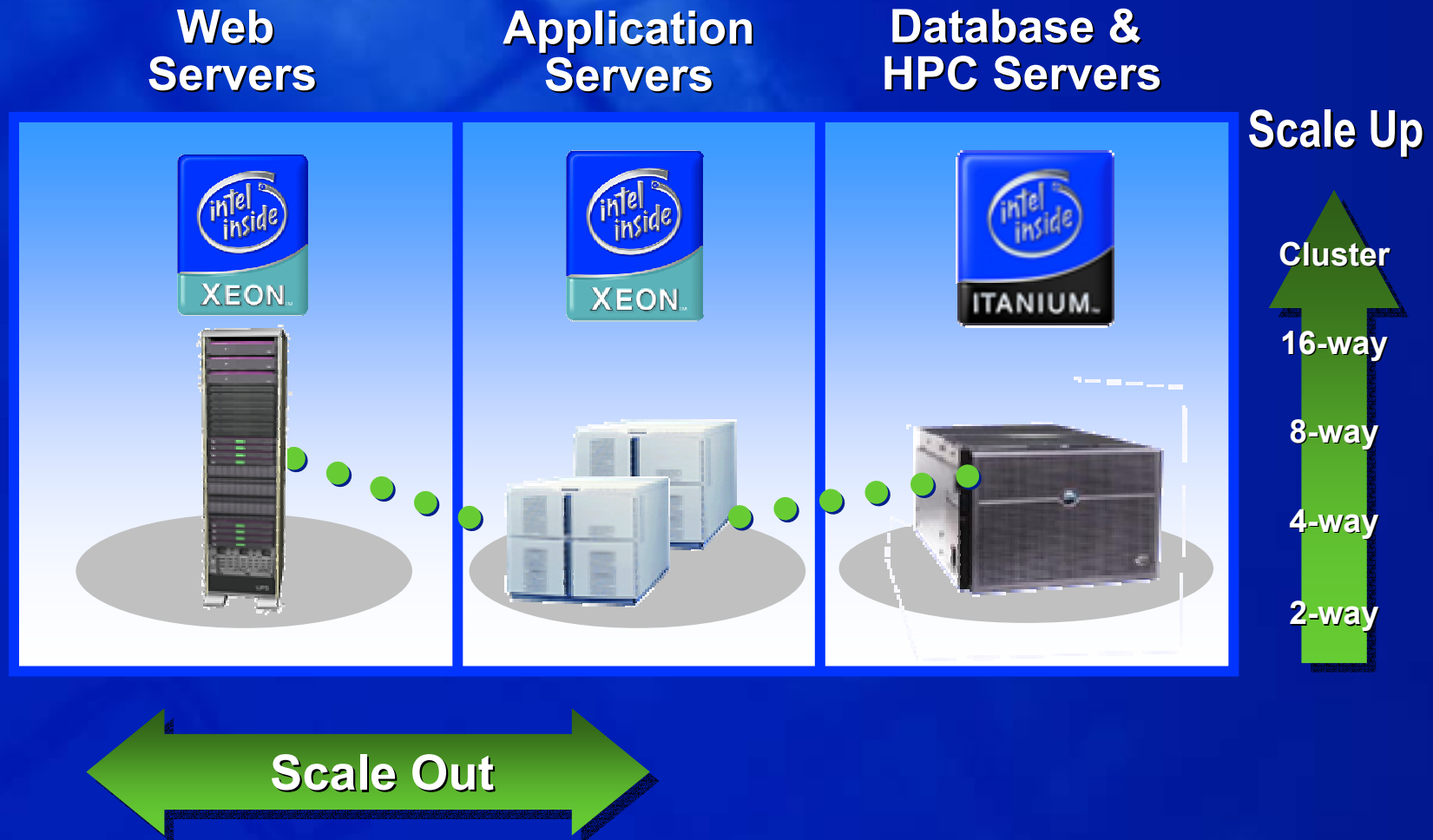
# Intel® Itanium™ Processor Family



- First 64-bit processor for the enterprise
- Design optimized for high-performance work-loads
- Hardware support for security
- McKinley – extending 64-bit price/performance

**Designed From Ground Up For High-end Enterprise**

# Scalable Enterprise Solutions On IA-32 & IPF Building Blocks



Demo

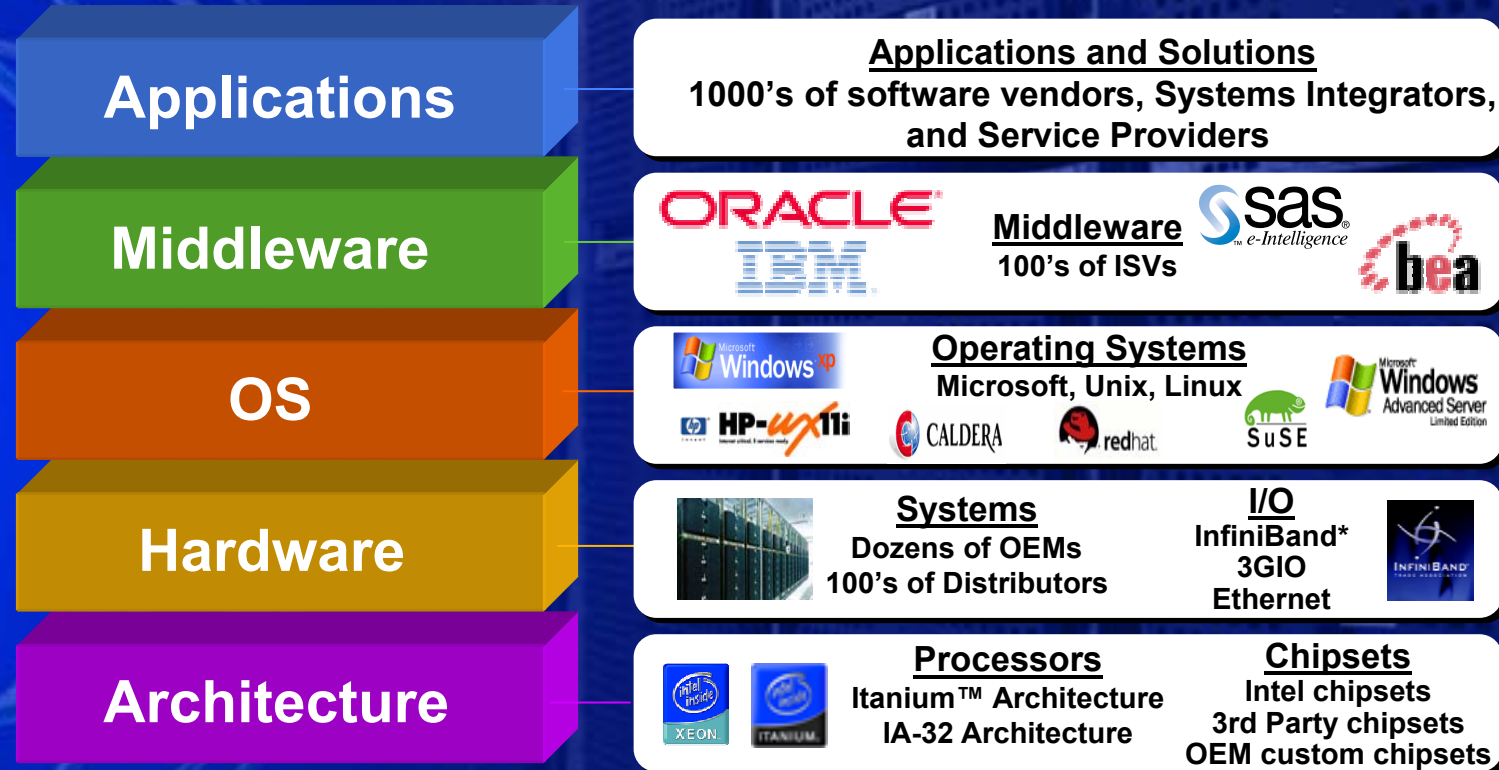
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# Broad Industry Support



Horizontal Solutions based on Common Architecture

\*Other names and brands are property of their respective owners.

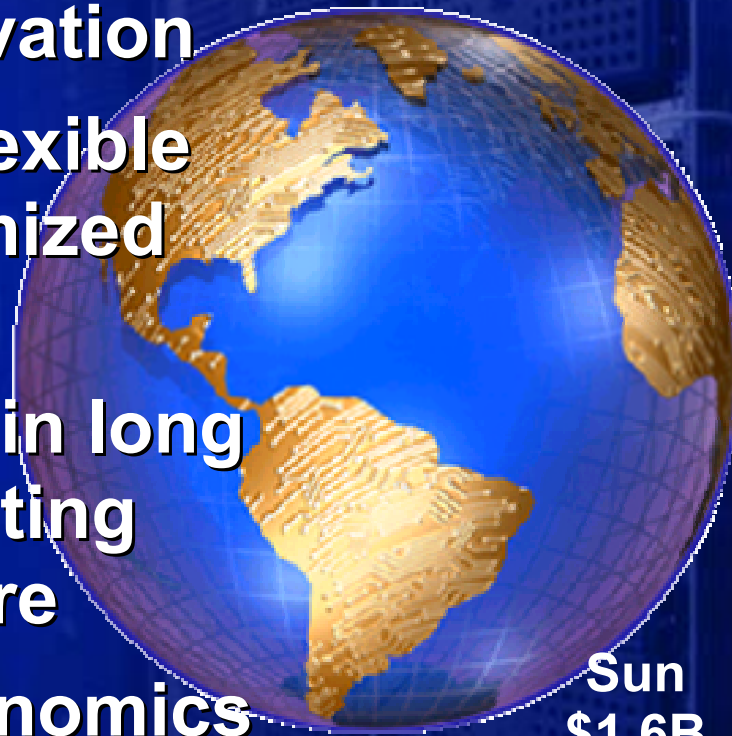
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**Intel Labs**

# Ecosystem of Intel-based Solutions Vendors

2000 R&D Spending (Billion \$)

- Faster innovation
- Choice of flexible AND customized solutions
- Confidence in long term computing infrastructure
- Volume economics



Some Major  
IA Vendors  
>\$19.0B\*

Sun  
\$1.6B

\* 2000 R&D spending for Intel, Microsoft, Compaq, Dell, HP, SGI & IBM; Source: 2000 Annual Reports

# Market Leaders on IA



**#1 Internet Portal, Over 1B Pages/Day**

**2nd Busiest Portal on the Internet**

**#1 Search Engine**

**Online Service: 300M page-views/day**

**Transactions: 2M/day; #1 Traded**

**e-Business: \$1B+ per month Online Rev.**

**Commerce: \$30M+ per Day**

**Online catalog: 4th Largest Site**

**Scale: 1.5M Users/Day, 2.5M @ peak**

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The Last 30 Years

Exponential Compute Performance Growth

***Intel Architecture:  
Fundamental  
Trajectory  
for The  
Technology Industries***

Performance

1970 1980 1990 2000 2010 2020

1 MPH

10 MPH

1000 MPH





# ***The Future***

**Extending & Expanding Moore's Law**



**“To God there is no zero.”**

Richard Matheson

***The Incredible Shrinking Man***

# Extending Moore's Law

**PERFORMANCE**

386

486



**Silicon Expertise**

**Architecture**

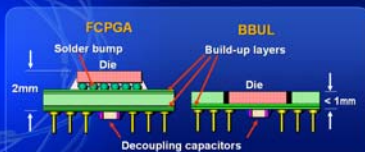
**Manufacturing**

**Delivering more MHz and MIPS to meet computing needs**

# Extending Moore's Law

## Technologies to Continue Meeting Computing Challenges

### Packaging Innovations: BBUL Bumpless Build-Up Layer



Intel Labs

### Extreme Ultraviolet Lithography (EUVL)

- Industry consortium for next-generation lithography – 1/20th wavelength
- 10-year effort
- Production in second half of decade

Industry First Reflective Mask for EUVL in 2001

Intel Labs

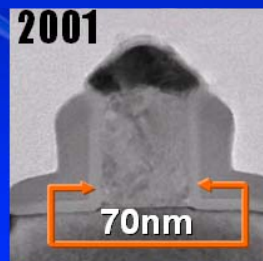
### Turbo-charging Computing with Intel® Hyper-Threading Technology



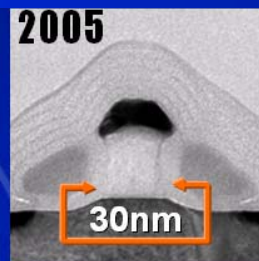
Intel Labs

## Intel: To the Terahertz Transistor

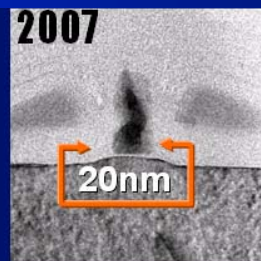
### Transistor Leadership Continues



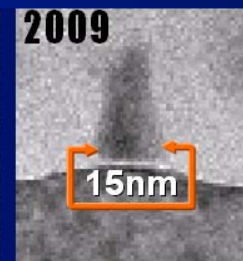
0.13µm process



65nm process

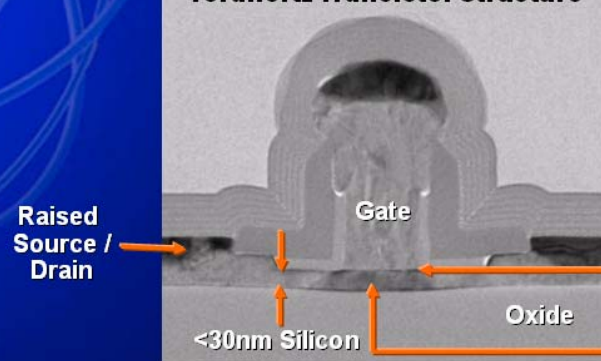


45nm process



32nm process

### Terahertz Transistor Structure



Source: Intel

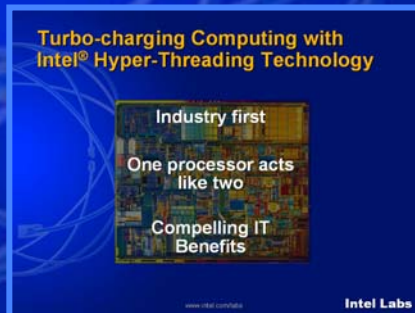
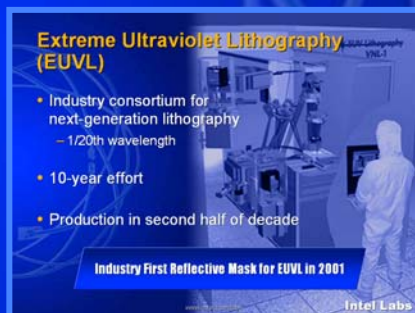
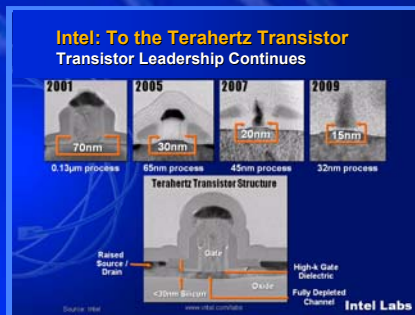
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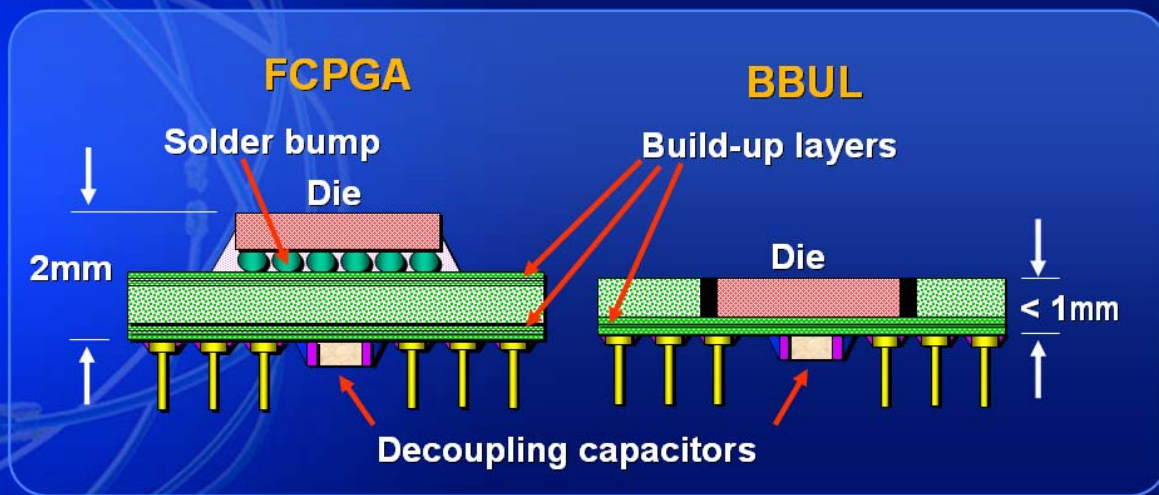


# Extending Moore's Law

## Technologies to Continue Meeting Computing Challenges



## Packaging Innovations: BBUL Bumpless Build-Up Layer

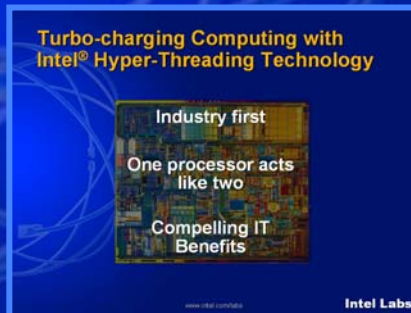
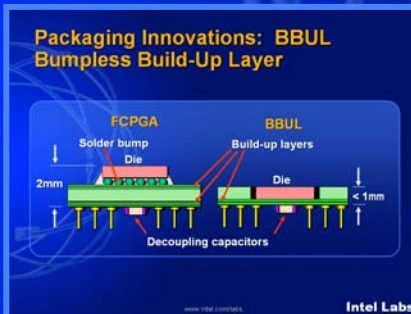
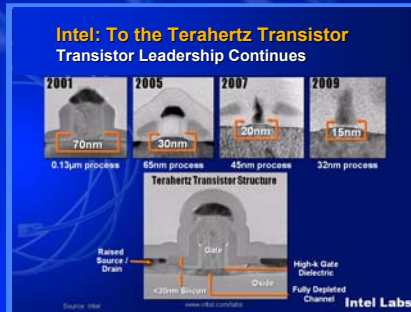


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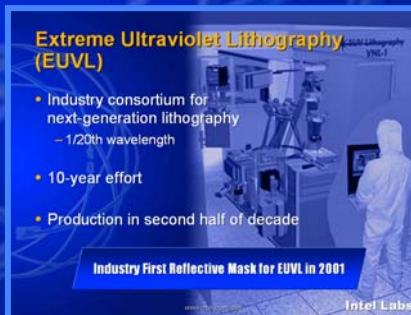
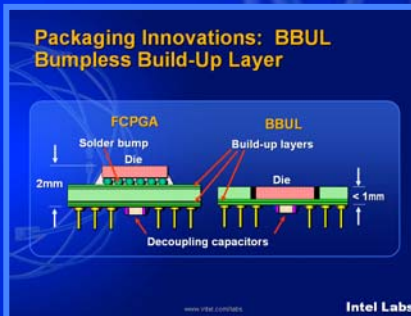
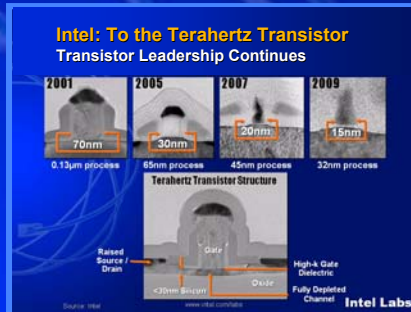
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**Intel Labs**

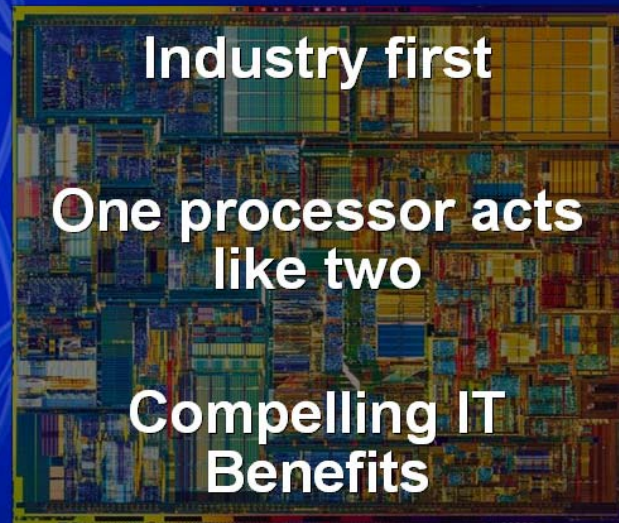


# Extending Moore's Law

## Technologies to Continue Meeting Computing Challenges



## Turbo-charging Computing with Intel® Hyper-Threading Technology



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**Intel Labs**

# The Result



30 GHz



5 GHz





# Expanding Moore's Law

**PERFORMANCE**

386 486



**Manufacturing**

**Architecture**

**Silicon  
Expertise**

**Delivering More MHz and More MIPS**

**Technologies  
to Keep  
on Delivering**

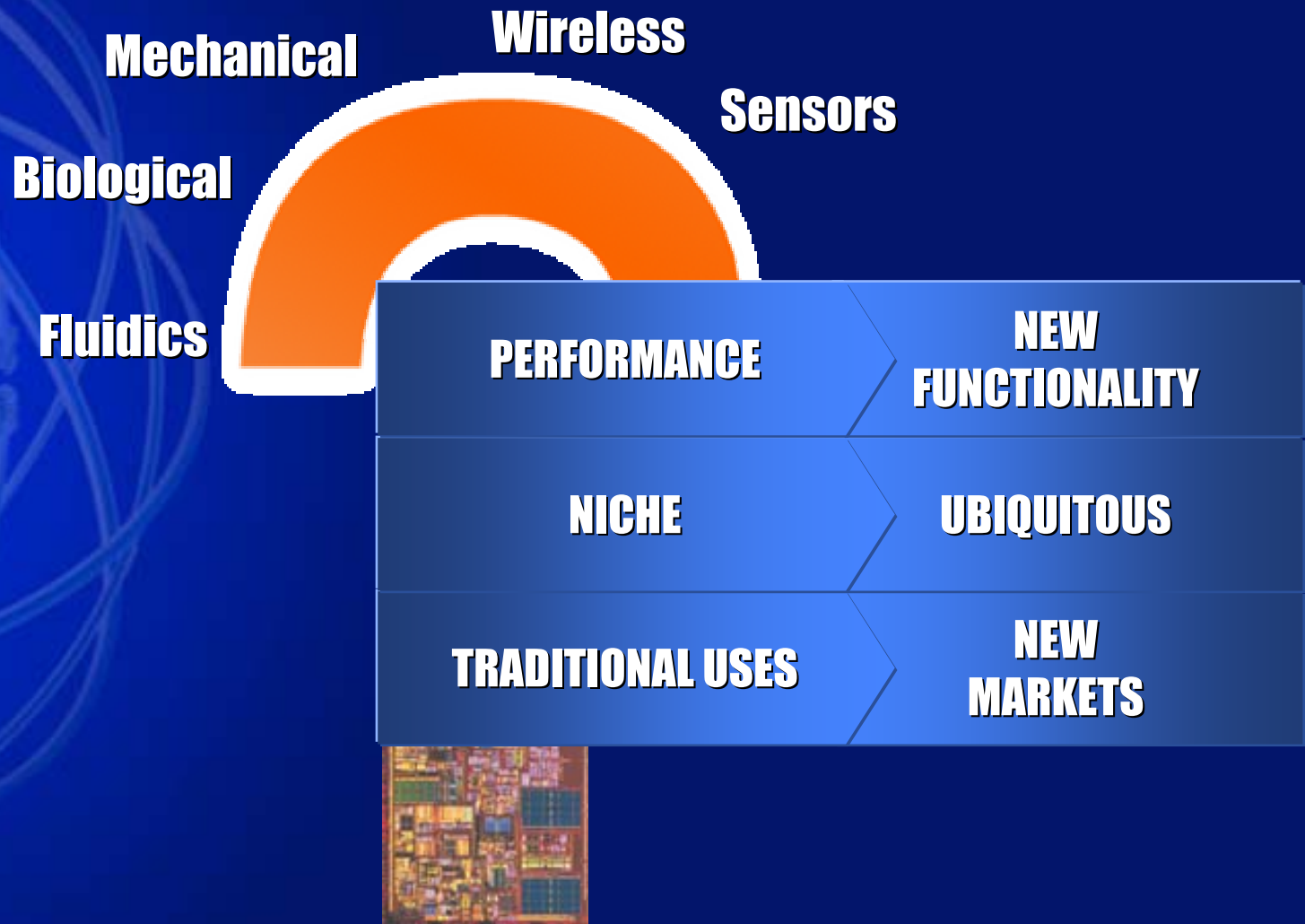


**Expanding Beyond  
Performance**

# Expanding Moore's Law

“... from *transistors*  
to *devices* ...”

# Expanding Moore's Law

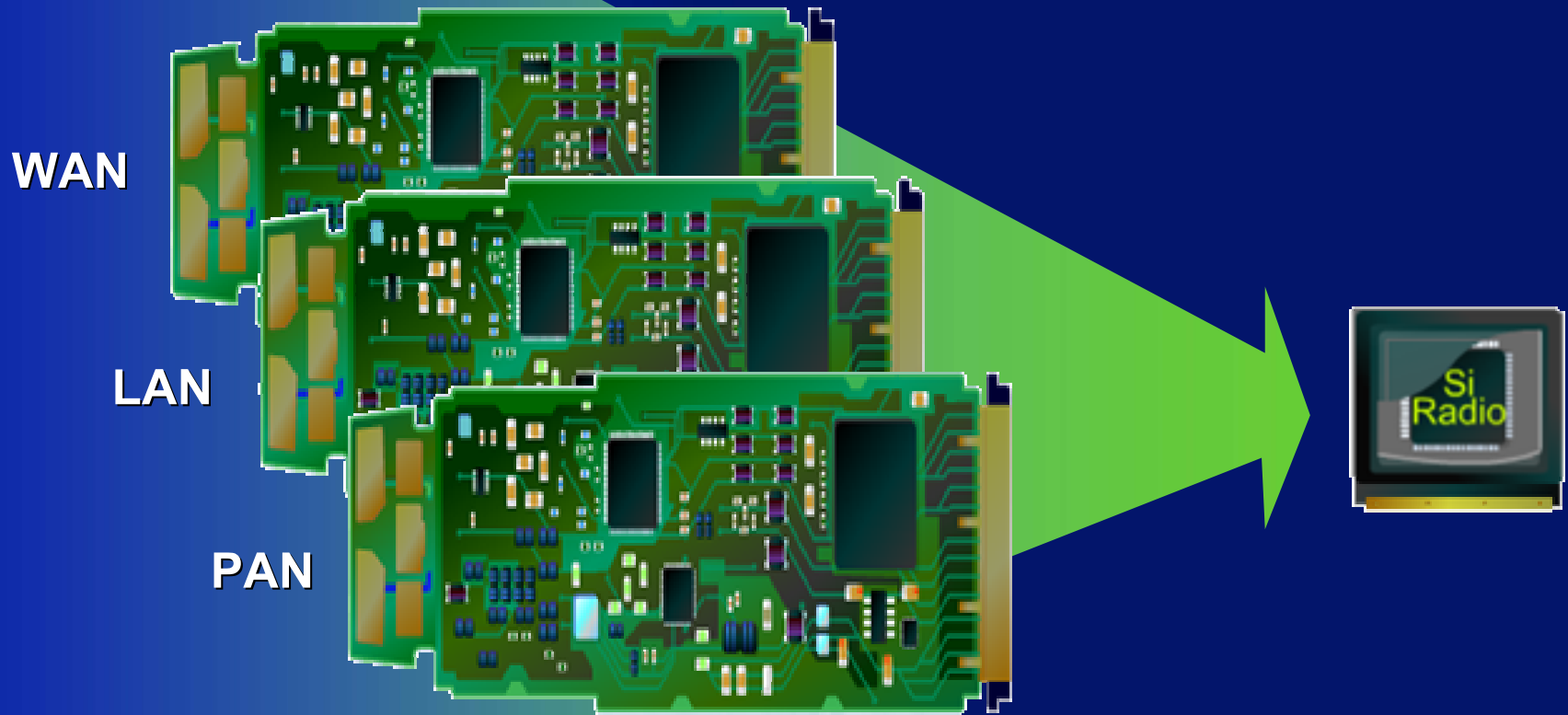




# ***“Radio Free Intel”***



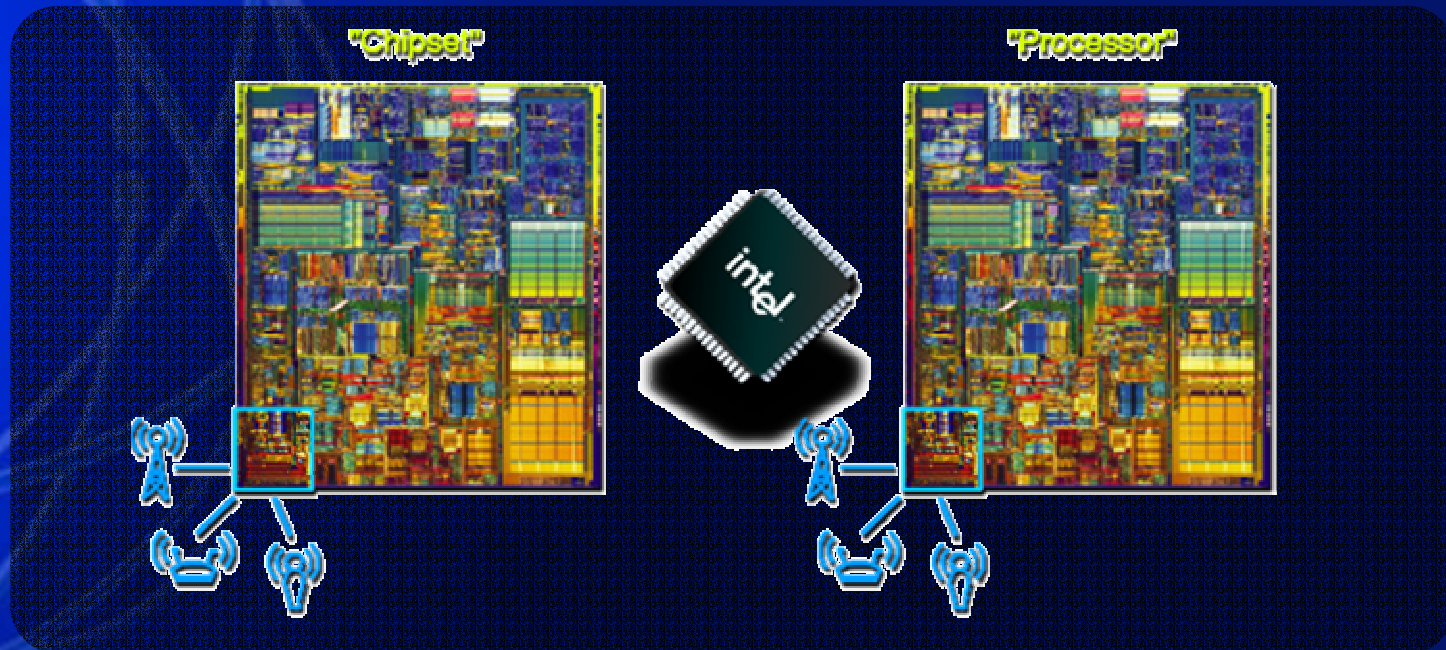
# Silicon Radio



**Converging Computing and Communications**

# When Radio Becomes “Free”

- Fully integrated
- Always connected
- Multiple networks



**the Vision**

# Devices of the Future



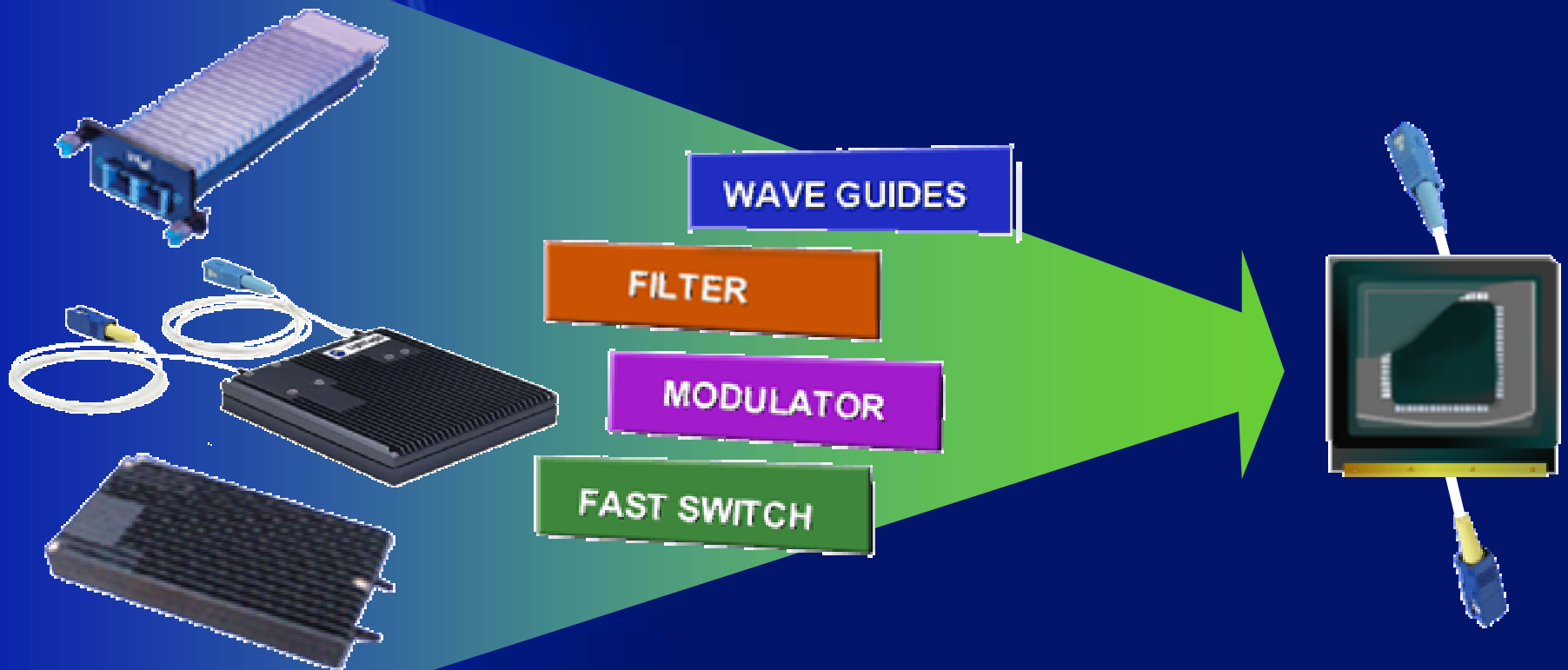


**Silicon Photonics**

***Photons Meet Electrons***



# Integrated Electronics and Photonics



**Silicon: Seeing the Light**





**METROPOLITAN AREA NETWORK**

**ENTERPRISE**

**DATA CENTER**

**RACK**

**CHIP**







**OBEY  
THE  
LAW**

**Invest in Intel Architecture**